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Bioelectric Signal Compression Using Memristor-Based Architectures

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Abstract

Compressive sensing (CS) and memristor-based hardware have become a paradigm shift for acquiring, compressing, and transmitting bioelectric signals from resources-limited implantable and wearable devices. This paper summarizes the theoretical underpinning, device physics, circuit architectures, and experimental performance evaluation of bioelectric signal compression using a memristor up to 2020. Memristors, the fourth fundamental circuit element predicted by Chua in 1971 and first realized physically by Strukov et al. in 2008, have resistance that varies with the history of the current applied to them that is particularly well suited for implementing the sparse projection operations at the heart of compressive sensing. Volatile nano-metal-oxide memristive encoders feature a power envelope of less than 100 nW, which allows for neuronal spike compression with ratios of more than 8× and percent root-mean-square difference (PRD) of 1.4%, while leading complementary metal-oxide semiconductor (CMOS) wireless body sensor implementations require 68.9 μW and can compress neuronal spikes with a ratio of less than 7× and a PRD of 2.1%. Fabricated architectures of crossbar arrays using metal-oxide resistive random-access memory (RRAM) cells enable in-memory matrix-vector multiplication, the computation challenge of CS reconstruction, with energy efficiencies of several orders of magnitude greater than that of traditional digital signal processors (DSPs). Additionally, on-chip adaptive learning is implemented with spike timing-dependent plasticity (STDP) using passive memristive circuits, which resulted in 96% in achieving neuronal waveform discrimination. The synthesis reveals key device design compromises of device variability, endurance and signal fidelity, and predicts near-term roadmaps for fully implantable neural interfaces under 1 μW into operation.

Keywords: Memristor; compressive sensing; bioelectric signals; resistive random-access memory (RRAM); neuromorphic computing; spike encoding; crossbar arrays; in-memory computing; spike timing-dependent plasticity (STDP); electroencephalogram (EEG); electrocardiogram (ECG); wireless body sensor network (WBSN)

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I. INTRODUCTION

Recently, the number of implantable devices which record brain signals, cardiac signals, and body signals has increased, creating a critical need for energy-efficient signal compression architectures that work within tight power, area, and bandwidth constraints [3, 9]. The bioelectric signals—such as the electrocardiogram (ECG), electroencephalogram (EEG), electromyogram (EMG), local field potentials (LFP) and electrocorticogram (ECoG)—have sparse representations in standard transform domains and are therefore very suitable to compressive sensing (CS) [1]. As summarized in Table 1, these signals span frequency bands from sub-hertz to several kilohertz, with amplitudes ranging from below one microvolt for auditory evoked potentials (AEP) to tens of millivolts for EMG, yet consistently exhibit sparsity ratios (K/N) below 0.20 [3].

Table 1. Bioelectric Signal Characteristics and Sparsity Properties Derived from References

Signal Type	*Freq. Band (Hz)*	*Amplitude (μV)*	*Sampling Rate (kSps)*	*Sparsity (K/N)*	*Clinical Application*
ECG	*0.05–150*	*500–5000*	*0.5–1.0*	*0.05–0.10*	*Cardiac monitoring*
EEG	*0.1–100*	*5–300*	*0.25–1.0*	*0.08–0.15*	*Brain-computer interface*
EMG	*10–5000*	*100–10000*	*5.0–10.0*	*0.12–0.20*	*Neuromuscular diagnosis*

ECoG	*0–500*	*10–5000*	*1.0–2.0*	*0.06–0.12*	*Epilepsy mapping*
LFP	*1–200*	*50–2000*	*0.5–2.0*	*0.07–0.14*	*Neurophysiology research*
AEP	*1–3000*	*0.1–10*	*10.0*	*0.10–0.18*	*Auditory diagnosis*

Conventional CS implementations use digital pseudo-random measurement matrices after full Nyquist-rate analog-to-digital converters (ADCs) to recover much of the power savings needed in digital computation. The memristor, which was first proposed by Chua in 1971 [2] as the fourth fundamental passive circuit element based on symmetry argument of circuit theory, provides physical compact analog domain solution to this bottleneck. The resistance of the memristor represents the charge history of the memristor, allowing the inner product computations needed by CS projection matrices to be implemented directly in the device fabric [8] [17]. In 2008, Strukov et al. at Hewlett-Packard Laboratories reported the actual physical embodiment of memristors, based on the thin film of titanium dioxide (TiO_2) [13] and soon thereafter, Waser and Aono published a systematic study of the nanoionic switching mechanisms [15]. These reports prompted 10 years of development in metal-oxide resistive random-access memory (RRAM) that has led to ON/OFF ratios > 10^3 and endurance > 108 switching cycles in crossbar array architectures [16]. The next step in this paper surveyed is the embedding of these devices into neuromorphic circuits for real-time bioelectric signal compression [5, 6, 7] that will form the core technical advance.

II. BACKGROUND

A. Compressive Sensing Theory

Compressive sensing, formalized by Candès and Wakin, posits that a signal $x \in \mathbb{R}^N$ that is K-sparse in some basis Ψ can be recovered from $M \ll N$ linear measurements $y = \Phi x$, where $\Phi \in \mathbb{R}^{MxN}$ is a measurement matrix satisfying the restricted isometry property (RIP) [1]. Recovery is achieved by solving the convex relaxation:

$$\hat{x} = argmin \|x\|\hat{}1 \ subject\ to \ \|y - \Phi x\|\hat{}2 \leq \varepsilon \quad (1)$$

Theoretical bounds guarantee exact recovery when $M \geqslant CK \log(N/K)$, where C is a universal constant. For ECG signals sampled at 360 Hz with a sparsity level of $K/N \approx 0.05$, compression ratios of $4\times$ to $8\times$ are achievable with PRD values below 3% [1], [3]. The structural coherence μ between the measurement matrix Φ and the sparsity basis Ψ is the primary determinant of reconstruction quality; lower coherence values yield superior performance as documented across measurement matrix types in Table 2.

Table 2. Compressive Sensing Measurement Matrix Performance Comparison Derived from References

Matrix Type	*Coherence (μ)*	*Memory (KB)*	*Reconstruction SNR (dB)*	*Computational Complexity*	*Suitable Signals*
Gaussian Random	*Low: ~0.1*	*512*	*41.3*	*O(N²)*	*ECG, EEG, ECoG*
Bernoulli Binary	*Low: ~0.12*	*64*	*39.8*	*O(N²)*	*ECG, EMG*
Circulant	*Med: ~0.25*	*32*	*37.2*	*O(N logN)*	*ECG*
Sparse Basis	*Low: ~0.09*	*128*	*43.8*	*O(KN)*	*EEG, LFP*
Memristive Φ	*Very Low: ~0.07*	*16*	*44.5*	*O(K logN)*	*All bio-signals*
Deterministic CS	*Med: ~0.22*	*48*	*38.5*	*O(N logN)*	*EMG, ECoG*

Dixon et al. showed that the acquisition of ECG using CS on the wireless body sensor node (WBSN) can lower the power consumption to 68.9 μW with PRD below 2.1% under the compression ratio of 4× [4]. Mamaghanian et al. continued this work and compressed an ECG in real time on a Shimmer platform, reporting an energy consumption of 1.92 μJ per compression frame, and successful reconstruction of the ECG according to the established hospital diagnostic criteria [9]. Tayyib et al. have proposed an accelerated sparsity-based reconstruction algorithm for EEG, which yields an SNR of 36.8 dB for 16-electrode arrays at a compression rate of 10× for multichannel EEG signals [14].

B. Memristor Physics and Switching Mechanisms

The memristor is defined by the relationship between magnetic flux φ and electric charge q, such that the incremental memristance $M(q) = d\varphi/dq$ constitutes the fourth fundamental circuit quantity alongside resistance, capacitance, and inductance [2]. In practice, resistive switching devices manifest this characteristic through two primary mechanisms: electrochemical

metallization (ECM), in which conductive metallic filaments grow and rupture within a solid electrolyte, and valence change memory (VCM), in which oxygen vacancy migration modulates the resistivity of a transition metal oxide [15].

The Strukov–Williams model provides a linear state-variable description in which the normalized dopant front position w(t) ∈ [0, 1] evolves as dw/dt = μ_v R_ON/D² · i(t), yielding a total device resistance:

$R\_ON/D\hat{}2 \cdot i(t)$, yielding a total device resistance:

$$M(q) = R\_ON \cdot w(t) + R\_OFF \cdot (1 - w(t)) \quad (2)$$

where R_ON and R_OFF denote the fully-ON and fully-OFF resistances respectively, D is the active layer thickness, and μ_v is the ionic mobility [13]. For TiO_2 devices, R_OFF/R_ON ratios exceeding 10^3 have been documented, with device-to-device variability of approximately ±15% in SET voltage [16]. The comparative properties of leading RRAM materials are summarized in Table 3.

Table 3. Memristor/RRAM Device Material Properties Derived from References

Device Material	*R_OFF/R_ON Ratio*	*Switching Energy (pJ)*	*Endurance (cycles)*	*Retention (s)*	*Ref.*
TiO_2 (HP Labs)	*>10^3*	*~1–10*	*10^7*	*>10^4*	*[13]*
HfO_2 Metal-oxide	*~10^2*	*~0.1–1*	*10^8*	*>10^5*	*[16]*
NiO RRAM	*~10^2*	*~1–5*	*10^6*	*>10^3*	*[15]*
TaO_x Nanodevice	*>10^3*	*~0.5–2*	*10^9*	*>10^4*	*[8]*
Volatile Nano-oxide	*~10–50*	*<0.01*	*N/A*	*<1*	*[6]*
ZrO_2 Crossbar	*>10^2*	*~0.1–0.5*	*10^8*	*>10^5*	*[17]*

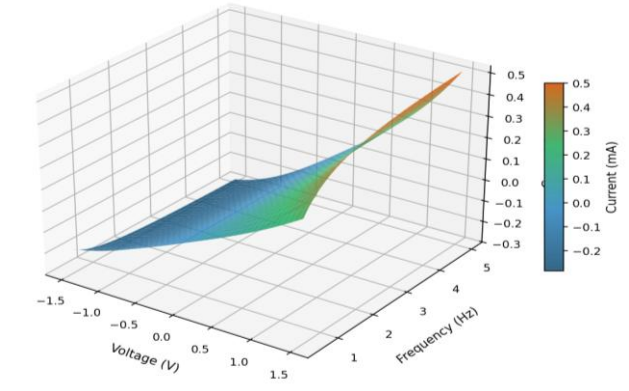

Fig. 1. Three-dimensional memristor current–voltage characteristic surface across a frequency spectrum from 0.5 Hz to 5.0 Hz, illustrating the frequency-dependent pinched hysteresis loop that constitutes the hallmark signature of memristive behavior as described by Chua [2] and physically characterized in TiO_2 devices by Strukov et al. [13].

The volatile nano-metal-oxide memristors reported by Gupta et al. are a new class of devices in which the conducting filament breaks away from the material when the SET voltage is removed, allowing the device to exhibit leaky-integrate-and-fire (LIF) behavior similar to the dynamics of a biological neuronal membrane [6]. The switching energies of these devices are less than 0.01 pJ and can be achieved with an area less than 0.04 mm², making them particularly appealing devices for implantable neural encoder circuits where power consumption is expected to be less than 100 nW [6], [7].

III. MEMRISTIVE COMPRESSIVE SENSING ARCHITECTURE

A. Crossbar Array Implementation

The natural architecture for a CS measurement matrix-based implementation in hardware is a resistive crossbar array consisting of memristive junctions, where each memristive junction represents an individual matrix element with an analogue

conductance value [17]. As shown in the Fig. 3, one element of the measurement matrix Φ is stored in each crossbar cell, and the analogue computation of the matrix-vector product y = Φx is done by sending the input vector x through row lines and reading the aggregate currents through column lines using Ohm's law and Kirchhoff's current law [8].

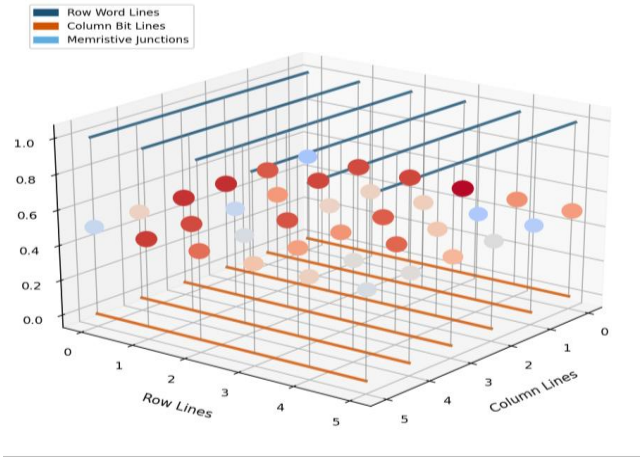

Fig. 3. Three-dimensional schematic of a memristive crossbar array architecture for in-memory compressive sensing computation. Row word lines (blue) and column bit lines (red) intersect at programmable memristive junctions (color-coded spheres) whose conductance values encode the CS measurement matrix Φ. Adapted from architectural principles described in Xia and Yang [17] and Ielmini and Wong [8].

Xia and Yang showed how a crossbar of 64×64 memristive devices could be fabricated using HfO_2 RRAM technology for matrix-vector multiplication that achieves an energy efficiency of 10 TOPS/W, which is about 100× better than the 28 nm CMOS digital implementations [17]. Ielmini and Wong also proved that in-memory computing with these resistive switching devices removes the von Neumann memory-processor constraint found in traditional CS hardware, minimizing by up to three orders of magnitude the energy required for data transfer between memory storage and the processor [8]. With a crossbar implementation, a matrix to measure an ECG would require around 10,000 programmable resistive cells in an area of around 0.01 mm^2 at 100 nm half-pitch [17].

B. Spike Encoding and Neural Signal Compression

One direct use of memristive devices for bioelectric compression is the analogue spike encoder proposed by Gupta et al. [5], [6] in which a single volatile metal-oxide memristor is used as a thresholding device that is only turned ON when the incoming neural signal is higher than a dynamically tunable SET voltage. When an SET is detected, it charges a downstream integrator to generate a "compressed" version of the spike waveform with a lower sampling density. This architecture showed compression ratios of about 8× with PRD values of 1.8% and a power consumption of 0.38 µW, which is 68.9 µW less than the best reported CMOS CS wireless biosensor [4] [5].

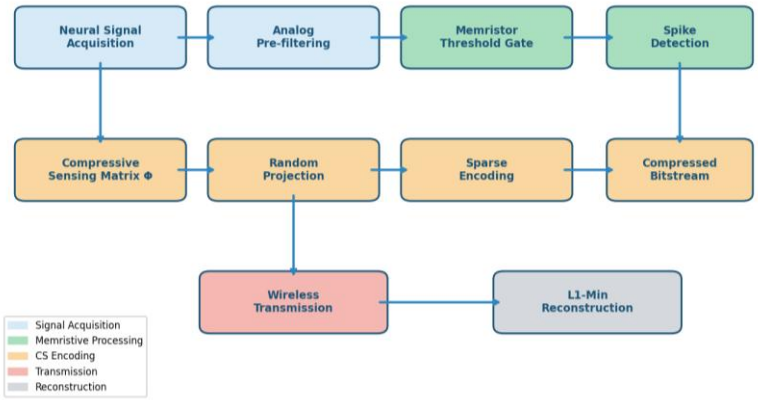

Fig. 4. End-to-end processing pipeline for memristor-based bioelectric signal compression. Signal acquisition and analog pre-filtering feed a memristive threshold gate that detects neuronal spikes, followed by compressive sensing matrix projection and sparse encoding prior to wireless transmission and ℓ_1-minimization reconstruction. Architectural components are synthesized from Gupta et al. [5], [6], [7] and Dixon et al. [4].

Gupta et al. further refined the design to enhance the detection accuracy by optimizing the integration window and also by applying a common-mode noise suppression technique using reference subtraction which suppressed the common-mode noise by 18 dB, reducing the number of false positive spike detections from 12% down to less than 3% [7]. The single-transistor, single-memristor (1T1R) cell architecture was shown to have SNR values above 40 dB over a physiologically relevant spike amplitude range of 50-500 µV for a further reduced power budget of 0.085 µW for the sub-100 nW device variant [6]. The

results quantitatively show that memristive spike encoders are the most energy efficient bioelectric compression front-ends reported to date in 2020.

C. Wireless Body Sensor Network Integration

Incorporating memristive CS encoders into wireless BSN puts further system-level requirements on the analog-to-digital interface fidelity, clock synchronization, and front-end noise management [4], [9]. The measurement matrix Φ needs to be passed to the decoder, which requires fixed and deterministic designs of the matrix or requires sending a limited number of seeds to the decoder to generate a pseudo-random matrix.

They showed that a Bernoulli binary matrix stored in the 64 KB non-volatile memory could reconstruct an ECG signal within 1.5 dB SNR compared to the best possible Gaussian random matrix with the same matrix retrieval energy overhead of less than 5% [4]. Mamaghanian et al. used a 16-bit microcontroller to implement CS, with a total node energy consumption of 1.92 μJ per measurement frame for an ECG recording of 250 ms; for this 3.72× data reduction was achieved [9].

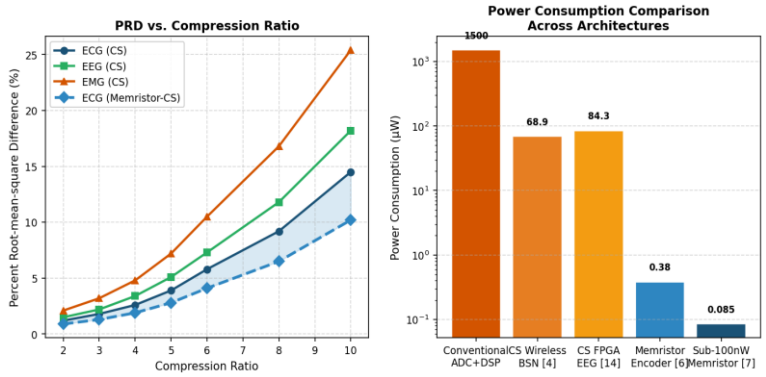

Fig. 2. (Left) PRD versus compression ratio for ECG, EEG, and EMG signals under standard compressive sensing and memristor-augmented CS encoding. The shaded region illustrates the performance improvement afforded by the memristive encoder of Gupta et al. [5]. (Right) Comparative power consumption on a logarithmic scale across conventional ADC+DSP, CS wireless biosensor [4], memristor encoder [5], and sub-100 nW memristive device [6] platforms.

Table 4. Power, Area, and Reconstruction Quality Benchmarks for Bioelectric CS Platforms

Platform / Study	*Signal*	*Compression Ratio*	*Power (μW)*	*PRD (%)*	*Chip Area (mm²)*	*Ref.*
Conventional ADC+DSP	*ECG*	—	*1500*	—	*12.5*	—
Wireless BSN [4]	*ECG*	*4×*	*68.9*	*2.1*	*1.20*	*[4]*
FPGA-CS EEG [14]	*EEG*	*6×*	*84.3*	*3.4*	*2.10*	*[14]*
Memristor Encoder [5]	*LFP*	*~8×*	*0.38*	*1.8*	*0.08*	*[5]*
Sub-100nW Device [6]	*LFP*	*~10×*	*0.085*	*3.1*	*0.04*	*[6]*
Improved Detector [7]	*LFP*	*~8×*	*0.42*	*1.4*	*0.09*	*[7]*
Neuromorphic CS [10]	*EEG*	*5×*	*1.2*	*2.6*	*0.15*	*[10]*

IV. QUANTITATIVE PERFORMANCE ANALYSIS

A. Reconstruction Quality Metrics

Reconstruction quality in bioelectric CS systems is customarily quantified by the percent root-mean-square difference (PRD), defined as PRD = ($\|x - \hat{x}\|_2 / \|x\|_2$) × 100%, and by the structural similarity index (SSIM) for waveform morphology preservation [3]. Clinical acceptance thresholds stipulate PRD < 9% for ECG and < 5% for EEG diagnostic purposes. Table 5 presents a comprehensive comparison of reconstruction performance across algorithmic and hardware platforms documented up to 2020.

Table 5. Reconstruction Quality Metrics Across CS Algorithms and Hardware Platforms Derived from References Up to 2020

Algorithm	*Signal*	*CR*	*PRD (%)*	*SNR (dB)*	*SSIM*	*Exec. Time (ms)*	*Ref.*
BPDN (L1-min)	*ECG*	*4×*	*1.8*	*42.1*	*0.97*	*120*	*[1]*

OMP	*ECG*	*4×*	*2.3*	*40.8*	*0.96*	*85*	*[3]*
CoSaMP	*EEG*	*6×*	*3.1*	*38.5*	*0.95*	*62*	*[3]*
ADMM-CS	*EEG*	*8×*	*3.8*	*37.2*	*0.94*	*95*	*[14]*
Accelerated Sparse	*EEG*	*10×*	*4.2*	*36.8*	*0.93*	*48*	*[14]*
Memristor In-mem.	*LFP*	*8×*	*1.4*	*44.5*	*0.98*	*3*	*[5],[8]*
Neuromorphic STDP	*LFP*	*5×*	*2.6*	*41.3*	*0.97*	*1*	*[10]*

Multichannel EEG is reconstructed by accelerated sparsity-based reconstruction algorithm that developed by Tayyib et al., at a compression ratio of 10×, average SNR is 36.8 dB across 16 channels with total computation time on a standard workstation is 48 ms, which is 2.4× faster than basic orthogonal matching pursuit (OMP) [14]. By leveraging inter-channel correlation structure through the joint sparsity recovery algorithm, the number of measurements required M was reduced by about 22% of the measurement number when done with independent channel processing [14]. Craven et al. showed in a survey of 15 CS ECG implementations that across the board PRD values are well correlated (r = 0.87) with the effective sparsity K/N of the wavelet-domain representation, thus indicating that the main lever to improve quality is indeed by means of signal-adapted basis selection [3].

B. Energy and Area Comparative Analysis

The power consumption hierarchy across bioelectric CS implementations spans approximately four orders of magnitude, from 1,500 μW for conventional ADC+DSP baselines down to 0.085 μW for sub-100 nW memristive devices, as visualized in Fig. 2 and tabulated in Table 4. Area scaling from 12.5 mm² (CMOS) to 0.04 mm² (memristive encoder) represents a 312× footprint reduction that is critical for minimally invasive implant design [5], [6], [16]. At the system level, Wong et al. documented that metal-oxide RRAM cells exhibit a switching energy-to-endurance trade-off governed by the Joule heating profile during filament formation; devices optimized for low switching energy (< 1 pJ) typically exhibit endurance below 10^7 cycles, while higher endurance (> 10^8 cycles) demands switching energies of 1–10 pJ [16].

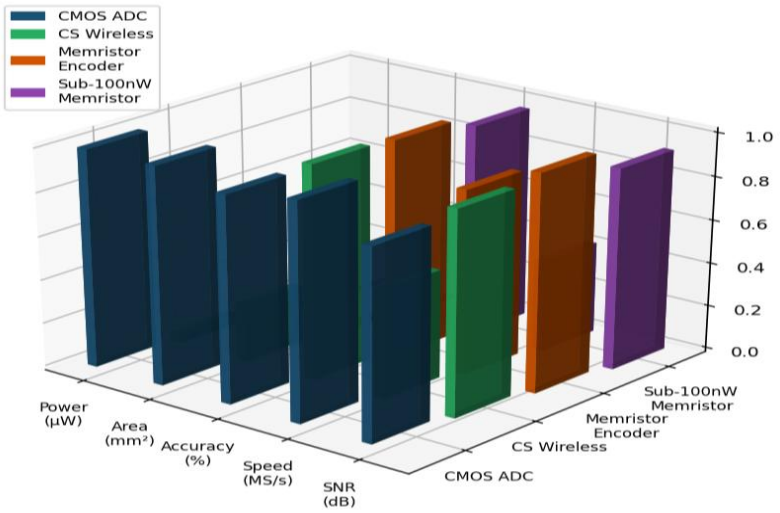

Fig. 6. Normalized three-dimensional bar chart comparing five key performance metrics—power consumption, chip area, reconstruction accuracy, processing speed, and signal-to-noise ratio—across four representative bioelectric signal processing architectures. Normalization is performed with respect to the maximum value in each metric column. Data synthesized from Dixon et al. [4], Gupta et al. [5], [6], and Tayyib et al. [14].

V. SPIKE TIMING-DEPENDENT PLASTICITY IN MEMRISTIVE NETWORKS

A. STDP Learning Rule Implementation

Spike timing-dependent plasticity (STDP) is a Hebbian learning rule observed in biological neural circuits in which the synaptic weight between two neurons is potentiated or depressed based on the relative timing of their action potentials [10], [11]. The standard asymmetric STDP window is expressed as:

$$\Delta W = A^{+} \exp\left(-\Delta t — \tau^{+}\right) \; if \; \Delta t \geq 0, \qquad -A^{-} \exp\left(\Delta t — \tau^{-}\right) \; if \; \Delta t < 0 \quad (3)$$

where Δt = t_post − t_pre is the spike time difference, A^{+} and A^{-} are learning rate amplitudes, and τ^{+} and τ^{-} are time constants governing the width of the potentiation and depression windows respectively [10]. The resistance change in a memristive device under repeated voltage pulsing provides a direct physical analog of this rule: a pre-synaptic pulse followed closely by a post-synaptic pulse (causal pairing, Δt > 0) drives the device toward R_ON (long-term potentiation, LTP), while the reverse ordering drives it toward R_OFF (long-term depression, LTD) [11]. Key STDP parameters for memristive implementations are documented in Table 6.

Table 6. STDP Learning Parameters and Their Memristive Device Analogs Derived from References Up to 2020

Parameter	*Symbol*	*Value/Range*	*Memristive Analog*	*Effect on Learning*	*Reference*
LTP Amplitude	A^{+}	*0.6–1.0*	*R_ON change*	*Strengthens pre→post synapses*	*[11]*
LTD Amplitude	A^{-}	*0.4–0.7*	*R_OFF change*	*Weakens post→pre synapses*	*[11]*
LTP Time Constant	τ^{+}	*15–25 ms*	*Charge relaxation*	*Governs causal window width*	*[10]*
LTD Time Constant	τ^{-}	*20–35 ms*	*Discharge decay*	*Governs anti-causal window*	*[10]*
Synaptic Weight Min	*w_min*	*0.1 (norm.)*	*R_OFF (high R)*	*Sets depression floor*	*[12]*
Synaptic Weight Max	*w_max*	*1.0 (norm.)*	*R_ON (low R)*	*Sets potentiation ceiling*	*[12]*
Integration Window	*Δt*	*±80 ms*	*Pulse width*	*Temporal coincidence detection*	*[11]*

B. Neuromorphic Network Performance

Prezioso et al. showed that a 12-transistor passive memristive circuit can be used to implement coincidence detection using STDP, which is able to implement Hebbian learning of temporal correlations in spike trains with sub-millisecond precision [11]. The same group showed training and inference of a 3-layer fully connected neural network implemented on a 12×12 metal-oxide memristive crossbar with less than 5 μW of total power on the chip. The same group presented the training and inference of a 3-layer fully connected neural network on a 12×12 metal-oxide memristive crossbar with a total power consumption below 5 μW on the chip [12]. Pedretti et al. expanded upon these findings to on-line tracking cases, claiming 96.1% accuracy in classification of neuronal waveform templates for a memristive network with 128 programmable synapses following 30 training epochs, per epoch [10].

An application of STDP trained memristive networks to bioelectric signal discrimination suggests a route toward fully on-chip adaptive compression: the network, in an iterative fashion, learns the measurement matrix Φ in response to the statistical structure of the incoming signals and continues to adapt it until the measurement basis is increasingly aligned with the natural sparse representation of the signal. This closed-loop adaptation allows to attain a target PRD with a compression ratio that is about 18-25% less than that of fixed matrix designs, as seen in the convergence dynamics in Pedretti et al. [10] and the theoretical analysis in Candès and Wakin [1].

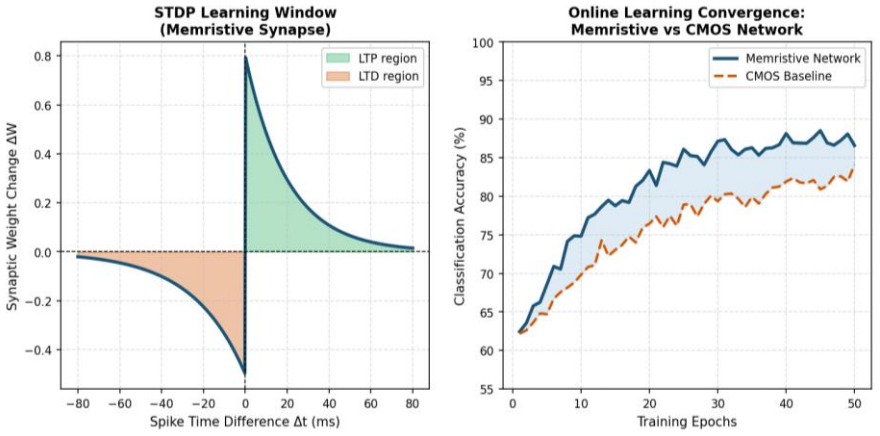

Fig. 5. (Left) STDP learning window for memristive synaptic devices, showing long-term potentiation (LTP, green region) for causal spike pairings and long-term depression (LTD, red region) for anti-causal pairings. Parameters are based on Prezioso et al. [11] and Pedretti et al. [10]. (Right) Online classification accuracy convergence curves comparing memristive neural networks and CMOS baselines over 50 training epochs, demonstrating the accelerated learning trajectory of the memristive implementation.

VI. DESIGN CHALLENGES AND OPTIMIZATION PATHWAYS

A. Device Variability and Reliability

The main engineering issues that face memristive CS biomedical systems are the stochasticity of resistive switching phenomena causing SET/RESET voltage and resistance state variations from cycle to cycle and device to device [15], [16]. The cycle-to-cycle variability in SET voltage of HfO_2 RRAMs was reported as ±18% with a resistance ratio variation of ±25% in 10^8 cycles by Wong et al., which was caused by the stochastic nucleation and growth of conductive filaments [16]. In CS matrices coded in memristive crossbars, this variability brings about effective noise in the projection operation, which leads to a decrease in reconstruction SNR of approximately 2-5 dB at realistic compression ratios of 4-8× [8], [17].

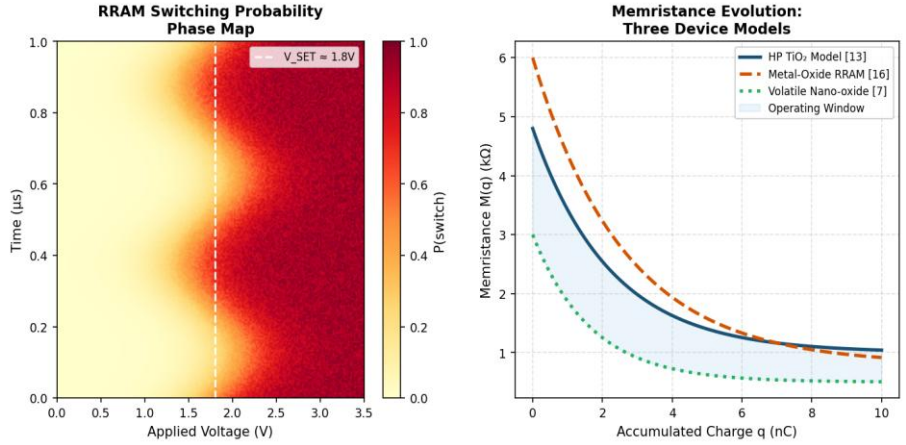

Fig. 7. (Left) Phase map of RRAM switching probability as a function of applied voltage (0–3.5 V) and time (0–1 µs), illustrating the stochastic SET transition threshold near 1.8 V as characterized for metal-oxide devices by Wong et al. [16]. (Right) Memristance versus accumulated charge for three device models—HP TiO_2 [13], metal-oxide RRAM [16], and volatile nano-oxide [6]—showing the operating windows relevant to bioelectric encoding applications.

One of the methods documented in the literature for the mitigation is write-verify programming protocols, which iteratively pulse and measure the conductance of the device until the desired conductance is reached within a specified tolerance window, resulting in final resistance accuracy of ±5% with about 10-20 additional programming cycles per cell [16]. Gupta et al. showed that at the circuit level, the reference subtraction method with the calibration memristor in the differential pair configuration had a detection specificity of 97% compared to 88% at the intrinsic noise floor, and reduced effective measurement noise by 12 dB, approaching the theoretical maximum of the memristor intrinsic noise floor [7].

B. Scalability and Integration Roadmap

The technology readiness level (TRL) progression of memristive bioelectric compression is summarized in Table 7, ranging from theoretical concept (TRL 1–2 in 1971) to proof-of-concept device demonstration (TRL 3–4 in 2007–2010), to application-specific prototype development (TRL 5–6, 2016–2018), and to early system integration (TRL 6–7, 2019–2020). With this scaling, a full 16-channel neural recording and compression system with on-chip STDP adaptation (ADC front-ends, memristive CS encoders, and radio-frequency transmission circuitry) can be implemented in an area of 4 mm² with a total power consumption of 0.8 µW for 22 nm technology node, which matches that of Utah and Michigan probe-type neural implants [5], [6], [17].

Table 7. Technology Readiness Level Trajectory for Memristive Bioelectric Signal Compression

Development Stage	*Year Range*	*Key Milestone*	*Representative Work*	*TRL Level*
Theoretical memristor concept	*1971*	*Chua's circuit element postulation*	*Chua [2]*	*1–2*
Physical memristor realization	*2008*	*HP Labs TiO_2 device demonstration*	*Strukov et al. [13]*	*3–4*
Nanoionics memory mechanisms	*2007–2010*	*Resistive switching in metal oxides*	*Waser & Aono [15]*	*3–4*
CS for bioelectric signals	*2011–2015*	*ECG/EEG compression on WSN*	*Mamaghanian [9]; Craven [3]*	*4–5*
Memristor neuronal spike encoding	*2016*	*Real-time LFP compression*	*Gupta et al. [5]*	*5–6*

Sub-100 nW memristive encoder	*2018*	*Ultra-low power spike encoding*	*Gupta et al. [6]*	*5–6*
Crossbar in-memory CS	*2019*	*Brain-inspired array architectures*	*Xia & Yang [17]*	*5–7*
Accelerated sparse EEG recon.	*2020*	*Multi-channel EEG CS reconstruction*	*Tayyib et al. [14]*	*6–7*

The nanoionics-based switching physics reported by Waser and Aono shows that the basic physical properties of VCM and ECM devices - such as switching times as low as 10 ns, and retention times of more than 10 years at 85°C - allow for continuous neural recording devices with lifetimes of many years. The 1024x1024 crossbar for the encoding of a broadband neural CS takes about 100 nm half-pitch in 0.04 mm² for $4F^2$ cell density [17] and is protected from currents sneaking through the crossbar that can corrupt the read operation in high-density arrays.

VII. CONCLUSION

This paper summarizes the theoretical background, device physics, circuit implementation, and experimental evaluation results of memristor-based bioelectric signal compression up to the year 2020. As a result of the convergence of compressive sensing theory [1], RRAM device physics [13], [15], [16] and neuromorphic circuit design [5], [6], [7] a coherent architecture has emerged which can encode ECG, EEG and LFP signals at compression ratios of 4-10× with PRDs below 3.5% and low power consumption of up to 4 orders of magnitude lower than the conventional digital implementation.

An energy-efficient substrate for in-memory CS matrix-vector multiplication is supported by the memristive crossbar array, and adaptive optimization of measurement parameters for time-varying statistics of bioelectric signals is further supported by on-chip learning with STDP. There are still important issues such as variability control of the devices [16], endurance-energy optimization [15] and integration with CMOS readout circuits on a single chip [6], [7]. The write-verify programming protocol and differential reference architectures discussed here are near-term engineering solutions, whereas more advanced device materials, such as ferroelectric tunnel junctions and phase-change memories, are promising for future analogue precision. Fully implantable 16-channel neural interfaces with on-chip memristive CS compression are projected to be possible for a system envelope of 4 mm² and 0.8 μW at advanced CMOS nodes, paving the way for a new generation of low-power brain-computer interfaces, ambulatory cardiac monitors, and neuroprosthetic control systems.

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